CLAIMS

1. A method of manufacturing a mechanically robust insulating layer, comprising:

forming a low-k dielectric layer having a first dielectric constant on a substrate; and

forming a carbon nitride cap layer on the low-k dielectric layer, the insulating layer thereby having a second dielectric constant that is less than the first dielectric constant.

2. The method of Claim 1 wherein a composition of the cap layer is C_xN_y, where x ranges between 0.1 and 0.9 and y ranges between about 0.1 and 0.9.

3. The method of Claim 1 wherein the low-k dielectric layer comprises a material selected from the group consisting of:

silicon dioxide;

hydrogen-doped silicon dioxide;

fluorine-doped silicon dioxide;

carbon-doped silicon dioxide; and

an organic polymer.

4. The method of Claim 1 wherein the carbon nitride cap layer is a first carbon nitride cap layer formed on a first major surface of the low-k dielectric layer and further comprising a second carbon nitride cap layer contacting a second major surface of the low-k dielectric layer.

5. The method of Claim 1 wherein the carbon nitride cap layer is formed by a process selected from the group consisting of:

ALD;

CVD;

PECVD; and

PVD.

6. The method of Claim 5 wherein the carbon nitride cap layer is formed by a process gas selected from the group consisting of:

C_2H_4;

CH_4; and

C_3H_8.

7. The method of Claim 5 wherein the carbon nitride cap layer is formed by a process gas selected from the group consisting of:

N_2;

NH_3; and

N_2H_4.

8. The method of Claim 5 wherein the process is PVD utilizing a target comprising a material selected from the group consisting of:

graphite;

azaadenine;

adnine; and

melamine.

9. The method of Claim 1 wherein the carbon nitride cap layer has a thickness ranging between about 50 Angstroms and about 800 Angstroms.

10. An integrated circuit device, comprising:

a substrate having at least one microelectronic device located therein; and

an insulating layer located over the substrate, including:

a thin-film, low-k dielectric layer having a first dielectric constant; and

a carbon nitride cap layer located on the low-k dielectric layer, the insulating layer thereby having a second dielectric constant that is less than the first dielectric constant.

11. The device of Claim 10 wherein the thin-film, low-k dielectric layer has a first hardness and the insulating layer has a second hardness that is greater than the first hardness.

12. The device of Claim 10 wherein the cap layer has a composition of C_xN_y, where x ranges between 0.1 and 0.9 and y ranges between about 0.1 and 0.9.

13. The device of Claim 10 wherein the low-k dielectric layer comprises a material selected from the group consisting of:

silicon dioxide;

hydrogen-doped silicon dioxide;

fluorine-doped silicon dioxide;

carbon-doped silicon dioxide; and

an organic polymer.

14. The device of Claim 10 wherein the carbon nitride cap layer is a first carbon nitride cap layer formed on a first major surface of the low-k dielectric layer and further comprising a second carbon nitride cap layer contacting a second major surface of the low-k dielectric layer.

15. The device of Claim 10 wherein the carbon nitride cap layer is formed by a process selected from the group consisting of:

ALD;

CVD;

PECVD; and

PVD.

16. The device of Claim 15 wherein the carbon nitride cap layer is formed by a process gas selected from the group consisting of:

C_2H_4;

CH_4; and

C_3H_8.

17. The device of Claim 15 wherein the carbon nitride cap layer is formed by a process gas selected from the group consisting of:

N_2;

NH_3; and

N_2H_4.

18. The device of Claim 15 wherein the process is PVD utilizing a target comprising a material selected from the group consisting of:

graphite;

azaadenine;

adnine; and

melamine.

19. The device of Claim 10 wherein the carbon nitride cap layer has a thickness ranging between about 50 Angstroms and about 800 Angstroms.

20. An integrated circuit device, comprising:

a first via contacting a microelectronic device in a substrate and extending through a first insulating layer located over the substrate;

a first trench contacting the first via and extending through a second insulating layer located over the first insulating layer;

a second via contacting the first trench and extending through a third insulating layer located over the second insulating layer; and

a second trench contacting the second via and extending through a fourth insulating layer located over the third insulating layer;

wherein at least one of the first, second, third and fourth insulating layers includes:

a dielectric layer having a first dielectric constant; and

a carbon nitride cap layer located on the dielectric layer, the at least one of the first, second, third and fourth insulating layers thereby having a second dielectric constant that is less than the first dielectric constant.

21. The device of Claim 20 wherein an etch stop layer interposes at least one pair of neighboring ones of the first, second, third and fourth insulating layers.

22. The device of Claim 20 wherein at least two of the first and second vias and the first and second trenches form at least one dual-damascene structure.

23. The device of Claim 20 further comprising at least one anti-reflective coating formed over one of the first, second, third and fourth insulating layers.

24. A semiconductor device, comprising:

a plurality of doped regions formed in a substrate; and

a plurality of isolation regions each proximate a junction of adjacent ones of the plurality of doped regions, wherein at least a portion of each of the plurality of isolation regions comprises carbon nitride.

25. A MEMs device, comprising:

a landing yoke configured to deflect in response to biasing thereof;

a mirror element coupled to the landing yoke; and

a control bus configured to bias the landing yoke;

wherein at least one of the landing yoke, mirror element and control bus includes a contact area coated with carbon nitride.